APPLICATION

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SERIAL DIGITAL COMMUNICATION SYSTEM AND METHOD

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SERIAL DIGITAL COMMUNICATION SYSTEM AND METHOD

This application claims the benefit of provisional patent application number 60/540,206 to Daly et al., filed January 28, 2004.

BACKGROUND OF THE INVENTION

Field of the Invention

This invention relates to the field of digital communication systems, and particularly to protocols for serial digital communication systems.

Description of the Related Art

Many systems exist for transferring data between peripheral devices and a master device such as a microprocessor. Such systems typically employ a multiple-wire bus structure to which each device is connected, with data transferred between devices either serially or in parallel. To retrieve data from a particular device on the bus, the device must first be addressed or enabled in some fashion.

One such system is known as the serial peripheral interface (SPI). The SPI is a full duplex, four wire synchronous serial interface based on a master/slave relationship. However, the SPI requires that each interconnected device have a pin by which the device is enabled prior to transferring data; this increases processing overhead and the system's I/O requirements. The system also requires 4 wires, which may consume more area than is desired.

SUMMARY OF THE INVENTION

A system and method for effecting serial digital communication is presented, which overcomes the problems

noted above. The present system requires just one wire, and none of the communicating devices requires an address.

The new system includes a master device having an input and an output, with a plurality of slave devices connected serially between the master device's output and input - thereby forming a closed chain. The system's protocol requires that each slave device transmit a predetermined number of pulse-width-modulated (PWM) pulses to the device immediately following it in the chain upon receipt of an end-of-transmission (EOT) signal from the device immediately preceding it in the chain, and to transmit an EOT signal when the transmission of its predetermined number of PWM pulses is completed. The master device is arranged to transmit an EOT signal to initiate the transmission of PWM pulses from each slave device.

Each of the slave devices passively buffers PWM pulses received from the device immediately preceding it in the chain, such that each device's PWM pulses are transmitted in one direction sequentially to the input of the master device via the intervening slave devices. Thus, upon transmitting the EOT signal, the master device receives a continuous stream of PWM pulses followed by a single EOT signal. In this manner, each device communicates in turn back to the master device, with each PWM pulse uniquely identified with its source device by its position in the incoming data stream.

In a preferred embodiment, each device responds to an EOT signal by transmitting a single PWM pulse, whose information content is coded in the ratio of the pulse's "high" time to its "low" time. The EOT signal is preferably a single narrow high pulse, whose total high time is less than the minimum permitted PWM pulse high time, and thus can be easily distinguished from the information passing through the chain.

An alternative protocol requires the slave devices to

transmit a "start-of-transmission" (SOT) signal prior to sending its PWM pulse(s). The SOT signals would be buffered by each slave device, and would serve to separate each device's PWM pulses.

Further features and advantages of the invention will be apparent to those skilled in the art from the following detailed description, taken together with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of a serial digital communication system per the present invention.

FIG. 2 is a timing diagram illustrating the operation of the system of FIG. 1.

FIG. 3 is a block/schematic diagram of one possible embodiment of a slave device per the present invention.

FIG. 4 is a timing diagram illustrating the operation of the slave device of FIG. 3.

FIG. 5 is a schematic diagram of one possible embodiment of a PWM pulse detector per the present invention.

FIG. 6 is a timing diagram illustrating the operation of the PWM pulse detector of FIG. 5.

FIG. 7 is a timing diagram illustrating an alternative operating protocol for a serial digital communication system per the present invention.

DETAILED DESCRIPTION OF THE INVENTION

A serial digital communication system per the present invention is shown in FIG. 1. A master device 10, such as a microprocessor or microcontroller, has an output terminal 12 and an input terminal 14. A plurality of slave devices (DEVICE 1, DEVICE 2,..., DEVICE N) are serially connected between the master device's output and input, thereby forming a closed chain. Each slave device has an input

terminal (IN) and an output terminal (OUT), with each input terminal connected to the output of the device preceding it in the chain, and each output terminal connected to the input of the following device.

The system is arranged to convey information via pulse-width-modulated (PWM) pulses, wherein information is coded in the ratio of the pulse's high time to its low time. Either analog or digital values can be encoded with the PWM pulse. For example, a temperature value could be encoded into a single PWM pulse, with the ratio of the pulse's high time to low time being proportional to the temperature. For digital encoding, one PWM duty ratio can be designated as a logic "0", with another duty ratio designated as a logic "1".

In a preferred embodiment, the system's protocol calls for each of the slave devices to transmit a predetermined number of PWM pulses to the device immediately following it in the chain upon receipt of an "end-of-transmission" (EOT) signal from the device immediately preceding it in the chain, and to transmit an EOT signal when the transmission of its predetermined number of PWM pulses is completed.

Transmission of PWM pulses from each device is initiated by master device 10, which transmits an EOT signal to the first device in the chain. Each slave device is arranged to passively buffer PWM pulses received from the slave device immediately preceding it in the chain. When so arranged, each device's PWM pulses are transmitted in one direction sequentially to the input of master device 10 via the intervening slave devices, such that, upon transmitting an EOT signal, master device 10 receives a continuous stream of PWM pulses followed by a single EOT signal.

An EOT signal comprises one or more pulses having characteristics which are clearly distinguishable from those of the PWM pulses. Preferably, the PWM pulses have a

defined minimum pulse "high" time, and each EOT signal is a single, high-going pulse having a pulse width which is less than the minimum pulse "high" time. Note, however, that there are numerous acceptable methods in which an EOT signal might be distinguished from the PWM pulses.

Operation of the serial digital communication system shown in FIG. 1 is illustrated in FIG. 2. Communication is initiated when master device 10 provides an EOT signal (a single pulse in this example) at its output. The first device in the chain, DEVICE 1, buffers the EOT pulse to its output pin, but when it senses the negative edge of the EOT pulse it starts transmitting the predetermined number of PWM pulses (one pulse in this example) - and so replaces the EOT pulse with a PWM pulse. As such, DEVICE 2 receives only the PWM pulse from DEVICE 1 (and not the EOT pulse), and buffers DEVICE 1's PWM pulse to the next slave device. DEVICE 1's PWM pulse is buffered in this way through all the remaining slave devices, and is delivered to master device 10 by the last device in the chain (DEVICE N).

After DEVICE 1 transmits its PWM pulse, it sends an EOT pulse. This acts as a terminator to the PWM signal (i.e., it indicates the end of the PWM pulse's "low" time), and triggers the next device - DEVICE 2 - to start transmitting its PWM pulse(s). Again, DEVICE 2 replaces the EOT pulse with its PWM pulse, which is buffered to master device 10 via the intervening slave devices.

When DEVICE 2's PWM pulse is complete, it transmits an EOT pulse which triggers DEVICE 3 to transmit its PWM pulse. Each slave device is triggered in this way until each has transmitted the predetermined number of PWM pulses.

The net result is that each slave device's PWM pulses are transmitted in one direction sequentially to the input of master device 10 via the intervening slave devices. Thus, after transmitting an EOT pulse to DEVICE 1, master

device 10 receives a continuous stream of PWM pulses followed by a single EOT pulse, with the first PWM pulse received by master device 10 being that sent by DEVICE 1, followed by that sent by DEVICE 2, etc. The last PWM pulse received, originating from DEVICE N, is immediately followed by an EOT pulse. To conserve power, each slave device may be arranged to be powered down after it has finished buffering incoming PWM pulses and transmitting its own PWM pulses and the EOT pulse.

The PWM pulses can be used to represent either analog or digital values. For example, the system can be arranged such that the duty ratio of a PWM pulse is proportional to an analog value, such as an IC's temperature or a particular voltage. Alternatively, a PWM pulse can be used to represent a binary value, with one duty ratio designated as a logic "0" and another duty ratio designated as a logic "1".

The slave devices can be arranged to transmit a single PWM pulse when triggered, or a predetermined number of PWM pulses. For example, to transmit 8-bit digital words, each slave device could be arranged to transmit 8 PWM pulses, with each pulse representing one bit of the word. Thus, either analog or digital data can be encoded as PWM pulses.

As noted above, each slave device sends a predetermined number of PWM pulses when triggered to transmit. In the simplest case, each device would transmit the same number of PWM pulses. However, the number of PWM pulses transmitted does not have to be the same for each slave device - as long as the system knows in advance how many pulses are transmitted by each device.

One possible embodiment of a slave device per the present invention is shown in FIG. 3, with its operation illustrated with the timing diagram shown in FIG. 4. In this example, the EOT signal is a single, high-going pulse with a predefined pulse width. The device includes a PWM

pulse detector 20, a PWM pulse generator 22, and a logic gate 24. A signal received at the device input (in this example, a PWM pulse 26) is applied to both PWM pulse detector 20 and PWM pulse generator 22. PWM pulse detector 20 toggles its output when the duration of the "high" portion of the incoming pulse exceeds the predefined pulse width of an EOT pulse - thereby indicating that the incoming pulse is a PWM pulse. When the detector output is high (28) (indicating that the incoming signal is a PWM pulse), the slave device is to simply buffer the incoming pulse. The detector output is connected to a reset input on PWM pulse generator 22, so that pulse generator 22 is prevented from generating its PWM pulse when the incoming signal is a PWM pulse (discussed in more detail below).

The input signal and the output of PWM pulse generator 22 are OR'd together using a logic gate 24. When PWM pulse generator 22 is inhibited, logic gate 24 passes the incoming PWM pulse on to the device output. The incoming PWM pulse is thus passively buffered to the following device in the chain.

PWM pulse generator 22 is preferably arranged to begin transmitting its PWM pulse whenever an incoming pulse is received. This is because the system does not know whether the incoming signal is a PWM pulse or an EOT signal until the predefined EOT signal width has been exceeded. Thus, PWM pulse generator 22 is arranged to assume that the incoming signal is an EOT pulse, and to begin transmitting its PWM pulse(s) on the incoming signal's positive-going edge - which it continues to do until PWM pulse detector 20 indicates that the incoming signal is a PWM pulse. This is seen in FIG. 4 with reference to pulse 29, which is the start of the PWM pulse from PWM pulse generator 22, but which is aborted when the output of PWM pulse detector 22 indicates that the incoming signal is a PWM pulse from a preceding device.

When an actual EOT pulse (30) is received, PWM pulse generator 22 begins and is permitted to continue transmitting its PWM pulse (32). This pulse is buffered to the following device in the chain via logic gate 24. After transmitting its PWM pulse, the device outputs an EOT pulse (34), which is also passed on to the following device in the chain via logic gate 24. In this way, each slave device buffers PWM pulses received from preceding devices, generates its own PWM pulses after determining that an incoming pulse is not a PWM pulse, and generates an EOT pulse after transmission of its PWM pulses is completed.

An exemplary embodiment of a PWM pulse detector 20 per the present invention is shown in FIG. 5, with its operation illustrated with the timing diagram shown in FIG. 6. The detector includes an input, which is connected to an RC network made from a resistor 40 having a resistance R and a capacitor 42 having a capacitance C; resistor 40 and capacitor 42 are connected together at a node "RC". The detector also includes a logic gate 44, the inputs of which are connected to the detector input and to node RC.

In operation, a high-going incoming pulse 46 causes node RC to increase at a rate determined by the RC network's time constant (=R*C). If the "high" portion of the incoming pulse is of sufficient duration, the voltage at node RC will increase until detected as a logic "high" by logic gate 44, thereby causing the detector's output to toggle high (and reset PWM pulse generator 22). However, the R*C time constant is set such that, if the incoming pulse is an EOT pulse, node RC will not increase to a logic "high" level, and the detector's output remains low.

Note that the slave device and PWM pulse detector implementations shown in FIGs. 3 and 5, and their corresponding timing diagrams in FIGs. 4 and 6, are merely exemplary. There are innumerable ways in which these circuits could be implemented to operate in accordance with

the present serial digital communication system.

In some applications, it may be advantageous to employ a protocol which uses a "start-of-transmission" (SOT) signal in addition to an EOT signal. An SOT signal would be generated by each slave device just prior to sending its PWM pulse(s). The SOT signals would be buffered by each slave device, and would serve to separate each device's PWM pulses.

Operation of the serial digital communication system shown in FIG. 1 using a SOT signal is illustrated in FIG. 7. Communication is initiated when master device 10 provides an EOT signal 50 (a single pulse in this example) at its output. DEVICE 1 responds by generating an SOT signal 52, followed by zero or more PWM pulses 54 (one in this example).

An SOT signal is preferably a pulse having a duty ratio different from that of either a PWM pulse or an EOT signal, so it may be distinguished from them by master device 10; in this example, an SOT pulse is distinguished by defining its "high" time as longer than the maximum allowed "high" time for a PWM pulse, and longer than an EOT signal. As before, DEVICE 1 transmits an EOT signal (here, a pulse 56) after sending its PWM pulse.

Upon receipt of EOT pulse 56, DEVICE 2 buffers the SOT and PWM pulse received from DEVICE 1, and then transmits its own SOT pulse 58, followed by its PWM pulse 60 and an EOT pulse 62. This sequence is repeated for each slave device in the chain. When the last slave device, DEVICE N, receives an EOT pulse from the preceding device, it sends an SOT pulse 64, followed by its PWM pulse 66 and an EOT pulse 68.

When so arranged, after initiating communications by sending an EOT pulse to DEVICE 1, master device 10 receives PWM pulses from each slave device, with each PWM pulse preceded by an SOT pulse, with a single EOT pulse at the

end of the data stream.

An advantage of using a SOT signal as described above is that each slave device need not transmit a pre-determined number of PWM pulses - each device can transmit any number of PWM pulses, including no PWM pulses. The master device will know which PWM pulses come from which device because each device's PWM pulses are preceded by a SOT signal. If a slave device is to transmit no PWM pulses, it would send just a SOT signal followed by an EOT signal.

While particular embodiments of the invention have been shown and described, numerous variations and alternate embodiments will occur to those skilled in the art. Accordingly, it is intended that the invention be limited only in terms of the appended claims.